

Comparison of the isolated and non isolated SEPIC converter

Jelena Milojković, Miljana Milić, Slobodan Bojanić, Octavio Nieto, Vančo Litovski

Abstract – A comparative study of the properties of the isolated and non-isolated SEPIC converter is given. That includes voltage gain, efficiency, and input and output impedance as functions of the duty cycle. To our best knowledge some of these properties were studied for the first time here.

Keywords - DC-to-DC converter, gain, duty cycle, efficiency, input impedance, output resistance

I. INTRODUCTION

The shortcut SEPIC stands for single-ended primary-inductor converter [1-3]. It is a variant of buck-boost converter enabling output voltages smaller and larger than the input voltage. It can be produced in a non-isolated version the schematic and the way of operation of which will be discussed in more details below and in an isolated version discussed later in less details. In that the two versions of the isolated converter will be considered with the turn ratio of the transformer taking values one and two.

The schematic of the non-isolated version has two versions of its own. These are depicted in Fig. 1. To simplify, only the first version will be studied with some details here. An example set of parameter values will be used as a driver of the developments. Since we are devoted to extraction and comparison of the properties, no theoretical developments or design formulas will be developed here. For these the reader is advised to visit [4].

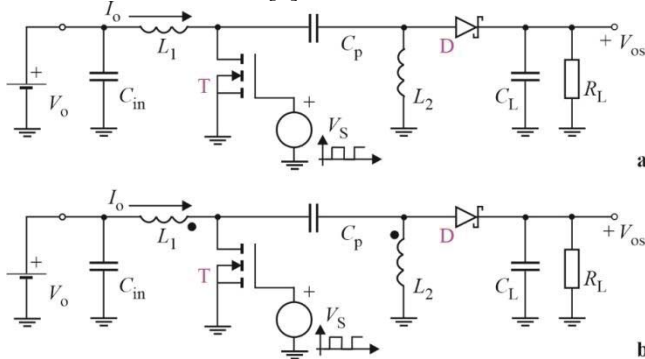


Fig. 1 Non-isolated version of the SEPIC converter. **a** Inductors are not mutually coupled and **b** inductors are mutually coupled

Jelena Milojković, Miljana Milić and Vančo Litovski are with Faculty of Electronic Engineering, Aleksandra Medvedeva, 4, 18000 Niš, Serbia, jelena.milojkovic@elfak.ni.ac.rs, miljana.milic@elfak.ni.ac.rs, vanco.litovski@elfak.ni.ac.rs; Slobodan Bojanić and Octavio Nieto Taladriz are with Universidad Politécnica de Madrid, Calle Ramiro de Maeztu, 7, 28040 Madrid, Spain, slobodan.bojanic@upm.es, octavio.nieto-taladriz@upm.es

From Fig. 1a we see that the main inductor (L_1) and the switch (T) are followed by a filter (L_2)- (C_p) and a rectifier (D) followed with a capacitive filter (C_L). These will play specific roles in the transfer of energy from the input (V_o) to the output (V_{os}). The number of passive elements being relatively large, one needs to pay much attention to the efficiency so that a Schottky diode is used instead of the one based on p-n junction.

Fig. 2 shows the SEPIC operating in continuous conduction mode (CCM). The top figure (a) depicts the on-state while the bottom (b) represents the off-state.

The study of the circuit's functionality will start by addressing the steady state condition of the on-state, (See Fig. 2a). The voltage on the inductor L_1 is equal to V_o . Assuming there was a residual charge in the capacitor C_p , the inductor L_2 takes energy from it. That is the fundamental novelty introduced by this topology: the capacitor is reinforcing the role of L_1 by temporarily transferring energy to L_2 . Hence, large value of C_p should be used. On the other side, C_L drives the output completely thanks to its own residual charge.

The operation in off-state is quiet more complicated. Now, since the diode is conducting, we have effective synergy of L_1 , C_p , and L_2 to recharge C_L and provide for the load. Note, in steady-state, since there is no change in the currents of both inductors, the average voltages across the inductors are zero. So, the average voltage across the capacitor C_p is equal to V_o . Of course, during transient, if C_p can be considered sufficiently large, one may neglect the AC component of the voltage across it.

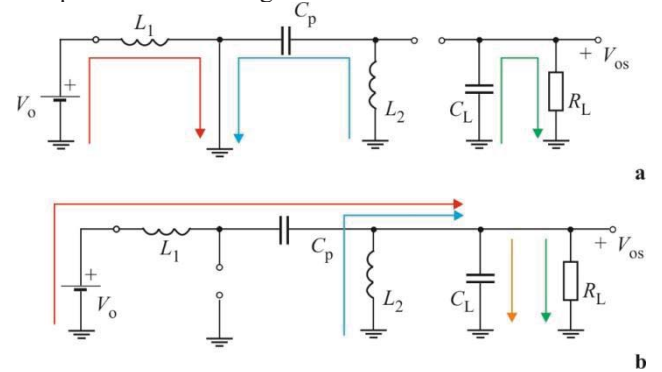


Fig. 2 SEPIC converter from Fig. 1 in steady states. **a** Currents in on-state and **b** currents in off-state

The isolated version of the SEPIC converter is obtained by substitution of the inductor L_2 (from Fig. 1) by a transformer. One expects that the secondary winding of the

transformer has larger number of turns so enabling boosting the output voltage. In that way a high-step up DC-to-DC converter is synthesized. The resulting schematic is depicted in Fig. 3. Note the ground terminal is connected to the part of the circuit related to the primary side of the converter. The part of the circuit related to the secondary side is expected to have its own reference terminal (zero voltage).

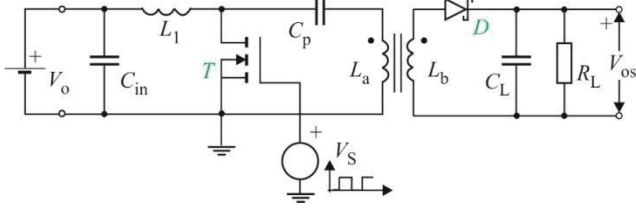


Fig. 3 Isolated SEPIC converter

II. COMPARISONS

The main difference between the two solutions is, of course, the DC isolation between the input and the output. In many cases this property is crucial for the proper operation of the converter. That enables control of the output DC voltage in addition to the one realized by the change of the duty cycle of the switching, extending the range of the output voltage to an even larger (for $n>1$) or smaller (for $n<1$) value, n being the transformer's turn ratio. The introduction of isolation, per se, brings in fore the issue of the reference potential of the load circuit. In other words the ground of the input voltage is separated from the ground of the load. This issue should be considered when PWM feedback is brought to the gate of the switching transistor. It also has to be isolated.

A specific property of the isolated SEPIC converter is that it can equally produce negative output voltage. For that to be accomplished the terminals of the diode should be swapped and the secondary winding of the transformer inverted.

Further we will extract the electrical properties of both solutions and represent in parallel.

First, the voltage gain will be considered. It is known from the literature [4] that

$$V_{os} = \frac{D}{1-D} V_o - V_D. \quad (1a)$$

or

$$\frac{V_{os}}{V_o} = \frac{D}{1-D} - \frac{V_D}{V_o}. \quad (1b)$$

where V_D stands for the voltage drop of a forward biased diode and D is the duty cycle of the switch. In the developing of this equation the switch and all passive elements were considered lossless.

Due to the losses (especially the switching losses of the VDMOS transistor) the gain of the real circuit deviates from this formula. That was verified by simulation the results being depicted in Fig. 4a.

Here two values of the load resistance were used while the duty cycle was varied from 0.1 to 0.9. The response of the non-isolated converter is denoted "NI" while the one of

the isolated by "I". $n=1$ was used. As can be seen that difference only arises for values of the duty cycle producing small value to either the pulse-width or the dip-width i.e. for low and high duty cycles, respectively. That may be attributed to the behavior of the transistor when traversing from on- to off-state and back. Namely, in addition to the change of the resistance of the transistor one has to charge and discharge the transistor's capacitances which are known to be large and nonlinear. In any case, the curves depicted are obeying equ. (1b) to a high extent.

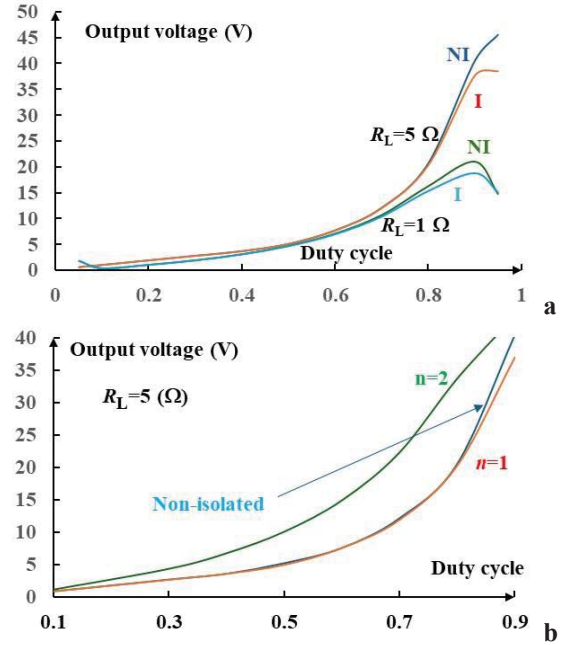


Fig. 4 (a) Output voltage as a function of duty cycle for two values of the load resistance. I stands for isolated ($n=1$) and NI for non-isolated and (b) the isolated case for $n=2$ included

Fig. 4b depicts the situation when $R_L = 5 \Omega$ and the curve corresponding to $n=2$ included. We can see that in a wide range of D the output voltage becomes doubled thanks to the new value of the transformer's turn ratio. Note, for a given output voltage of the converter one will need seriously different values of D for the two cases ($n=1$ and $n=2$). So, one may avoid using large values of D when large output voltages are needed to be produced.

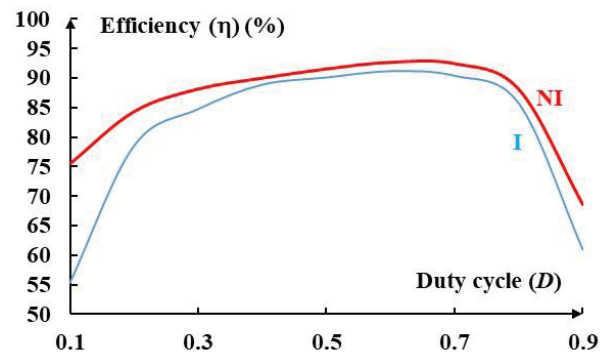


Fig. 5 Efficiency as a function of the duty cycle. I stands for isolated ($n=1$) and NI for non-isolated

Next the efficiencies will be compared. The results

represented in Fig. 5 are affected by the losses in the transistor and the diode only. All passive elements are considered ideal. The curves were obtained by repetitive simulations of both circuit. The way of how the efficiency was extracted, however, differs. For the non-isolate case the consumed energy per period was used while for the isolated case the DC components were introduced into the power formulas ($p=v \cdot i$) which were consequently divided.

In any case the results confirm the high value of the efficiency in a wide range of values of the duty cycle. The difference between the traces comes from the (error prone) way of extraction of the voltages, currents and energy from the Spice responses.

Note, the efficiency of the isolated converter for $n=2$ is not shown since no new sources of losses were introduced. Input impedance is rarely, if at all, studied for this kind of circuits. Its importance, however, comes in fore when multistage processing of the DC voltage occurs. For example, if the origin of the power is the mains, than the DC-to-DC converter will follow the rectifier/filter which is providing an unregulated DC voltage. The design of the filter is crucially affected by its load resistance which, in this case, is the input resistance of the converter.

Generally speaking, here, the DC input resistance is of interest. It is defined by

$$R_{in} = V_o / I_o. \quad (2)$$

After repetitive simulations of both circuits the diagram depicted in Fig. 6 was created. It represents the DC input resistance as a function of the duty cycle for the non-isolated (green line) the isolated for $n=1$ (overlapped with the previous) and the isolated for $n=2$ (blue line). Note, the input voltage was held at $V_o = 5V$ all the time.

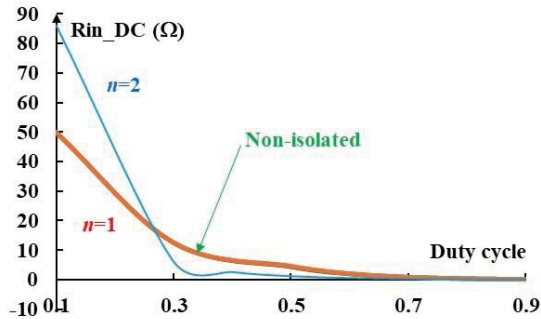


Fig. 6 DC input resistance. The non-isolated and the isolated cases for $n=1$ overlap.

By studying this diagram we notice the strong dependence of the input resistance on the duty cycle for both the isolated and the non-isolated case. This means that the designer of the previous stage must be aware of the value of D used in the converter and so accommodate the design.

Rising the turn ratio of the embedded transformer when $n > 1$ (what is the case here) boost the output voltage as seen from Fig. 4b. The input current of the transformer experiences the same. That means that the DC component of the overall input current will be risen too. For a fixed input DC voltage that will lead to reduction of the input resistance.

One frequently encounters in the literature a (small

signal) frequency domain analysis of the switching mode converters. Since, in fact, by the switching two linear circuits are created alternatively, one uses averaging of the signal and single frequency response is created. We do not support such way of thinking since while switching the topology of the circuit gets fundamentally changed. That may be seen from Fig. 2 where the residual linear circuits of the non-isolated SEPIC converter are depicted.

So, to enable frequency domain characterization we propose two simulations to be done: one for the on-state and the other for the off-state. To enable this we first introduce a sinusoidal voltage source in series with V_o (Fig. 1). Then, the first circuit (on-state) is created by setting a fixed value of the gate voltage (here $V_G = 12V$) while the second one by putting $V_G = 0$. Note, the Spice simulator, to start the simulation, creates linear models of the nonlinear elements (transistor and diode) for the biasing given. That means no ideal short-circuit or open-circuit is present in any of the frequency domain equivalent circuits.

This method was implemented to study the input impedance of the inverter. The simulation results are depicted in Fig. 7.

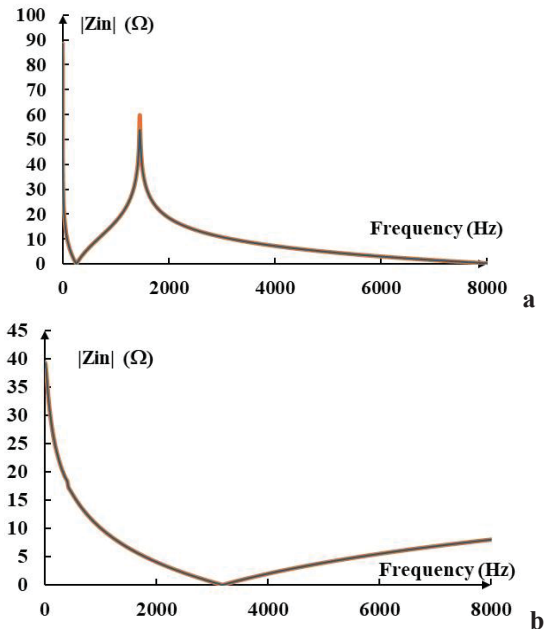


Fig. 7 Modulus of the input impedance as a function of frequency. (a) for off-state and (b) for on-state. Isolated ($n=1$) and non-isolated overlap.

From both parts of the circuit we recognize that the introduction of the transformer did not affect the input impedance. It stays equal for both circuits. The shape of the dependence, however, differs significantly. The input impedance when off-state is active has two resonance frequencies which means (for components of the input signal at these frequencies) it represents a short and open circuit at the input. The input impedance of the on-state has only one resonance frequency which differs from the ones existing for the off-state. We conclude here that the converter behaves as a filter for some of the components of the input signal but not all the time of switching.

We will finish the proceedings by a study of the output resistance. The importance of the output resistance comes in fore when accommodation to the load is sought. Of course, the load may be some additional electronics such as inverter producing AC voltage at the output. Since voltage is produced, however, minimum output resistance is preferred.

The issue of extracting the output resistance from the output waveform imposes two simulations for two values of the load resistance being very near to each other. It assumes linear operation for small increments and uses the model of the output circuit depicted in Fig. 8. Here the active part of the converter is represented by a VCVS ($A \cdot V_o$) where the gain A is unknown. Then the output resistance (R_{out}) of the converter completes the “macromodel” of the output.

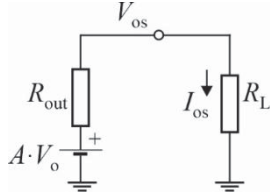


Fig. 8 Calculation of the output resistance of a converter

For this circuit one may write

$$V_{os} = \frac{R_L}{R_L + R_{out}} \cdot A \cdot V_o \quad (3)$$

After two simulations of the converter were performed for R_{L1} and R_{L2} two respective DC output voltages V_{os1} and V_{os2} were obtained. By substituting the values of these quantities in (3) one gets two linear equation with A and R_{out} as unknown. Solving this system of equations for R_{out} gives:

$$R_{out} = \frac{R_{L1}R_{L2}(V_{os2} - V_{os1})}{R_{L2}V_{os1} - R_{L1}V_{os2}}. \quad (4)$$

This formula performs division of two subtractions. Numerically speaking it is very error prone especially when small uncertain values are manipulated. The problem is the values of the voltages are similar as are the resistances so small errors in reading of the voltages from the screen representing the response leads to significant errors when the voltages are small as such. That is why we will represent here the values of the resistances for $D > 0.5$ only.

Repetitive simulations were performed to get the dependence of the output resistance on D based on (4). The results are depicted in Fig. 9. We notice that the values of the output resistances of the non-isolated and the isolated ($n=1$) converters are similar while the output resistance of the isolated converter ($n=2$) at low values of D is seriously reduced. Note, the output resistance never takes negative values.

The one depicted in Fig. 9 is consequence of the Excel's interpolation algorithm. When observing these traces on must be aware of that, as depicted in Fig. 4b, different values of D (for $n=2$) lead to different values of the output voltage.

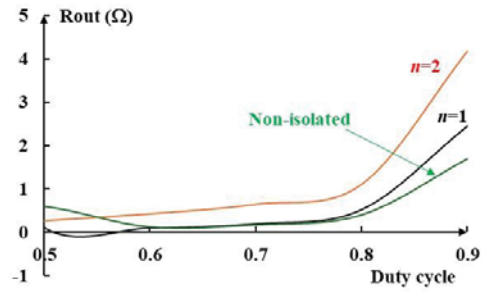


Fig. 9 Output resistance as a function of the duty cycle

III. CONCLUSION

Two version of the SEPIC converter's topologies were studied in parallel namely the non-isolated and the isolated the later taking two values for the transformer ratio $n=1$ and $n=2$. The gain as a function of the duty cycle and the load resistance was considered first. Then the efficiency was calculated as a function of the duty cycle. Almost identical behavior for non-isolated and the isolated with $n=1$ was observed. The case $n=2$, of course, produces larger gain. It is not shown here but the case $n=0.5$ behaves in accordance with the above considerations: the gain is smaller. Specific of these proceedings are the studies of the input and output resistances of the converter. It was shown that the non-isolated and the isolated for $n=1$ exhibit very similar properties in this aspect too. Changing the value of n will affect both the input and the output resistances, reducing the first and rising the second one.

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